

Low-cost wafer bumping

As the demand for flip-chip interconnects mounts across an increasingly large spectrum of products and technologies, several wafer-bumping processes have been developed to produce the small solder features required for this interconnect technology. These processes differ significantly in complexity and commensurate cost. Recently, a new bumping process developed at IBM Research called injection-molded solder, or IMS, has shown the capability to combine low-cost attributes with high-end capabilities. The development of IMS technology was driven by the need to reduce wafer-bumping costs while simultaneously addressing the conflicting needs of increasing wafer dimensions to 300 mm, decreasing bump and pitch dimensions below 75 μm on 150- μm centers, and optimal Pb-free alloy selection and processing. This paper describes IMS technology for both standard eutectic SnPb and Pb-free wafer bumping. Existing mainstream bumping technologies are also reviewed, with a focus on the challenges of new industry requirements. Early manufacturing challenges are addressed, including solutions that demonstrated the appropriateness of IMS technology for low-cost 300-mm Pb and Pb-free wafer bumping. Early process and reliability data are also reviewed.

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Introduction

Flip-chip solder-bump interconnection, the face-down soldering of integrated circuit (IC) devices to chip carriers, has been in manufacturing for nearly forty years [1]. First introduced in 1964 with the solid logic technology in the IBM System/360*, it was designed to extend interconnection capabilities beyond the existing wire-bonding techniques [2]. Unlike wire bonding, the area array solder-bump configuration allows the entire surface of the chip (die) to be populated with solder bumps that are subsequently interconnected to a substrate by the C4 (controlled collapse chip connection) solder reflow process for the highest possible I/O counts in order to meet the ever-increasing demand for electrical functionality and reliability in IC technology. Although wire bond still dominates IC interconnects in terms of absolute numbers, flip-chip packaging is poised for continued strong growth as it gains in many applications previously dominated by wire-bond technology, due primarily to the improvements afforded by C4 in such aspects as electrical performance, functionality, and reliability.

The various technologies that exist for depositing these tiny solder bumps on IC devices at the wafer level are known as solder wafer bumping and, more specifically within IBM, C4 wafer bumping. The original wafer-bumping technique of metal mask evaporation, in which both the ball-limiting metallurgy (BLM) [or under-bump metallurgy (UBM)] and solder are evaporated through mask holes in an area array fashion onto the wafer surface, was first developed and perfected by IBM nearly forty years ago. However, as the needs for increased I/O density and total I/O count are intertwined with the constant pressures to lower the cost of flip-chip interconnections, other wafer-bumping techniques have been developed. Electroplating of solder bumps has seen success in areas demanding higher density, while stencil-printing/paste-screening techniques are being adopted in cost-sensitive applications [3].

Today, important major trends in the industry, in conjunction with continued demands for both higher density and lower cost, are converging to a point at which the transition to a new bumping technology may be both opportune and necessary. First, in response to both governmental regulations and customer demands, the

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electronics packaging industry is in the process of making a major transition from PbSn to Pb-free solders. This introduces a new challenge: The bumping process must be generally compatible with this solder transition; also, since the optimal Pb-free alloy is still in the process of being selected, the bumping process must be able to accommodate various potential Pb-free solder compositions. Second, the recent transition from 200-mm to 300-mm wafers requires a bumping process that can readily accommodate this nearly 125% area increase with no negative effect on bumping yields and/or overall bump quality.

The bumping technologies in existence today address these trends with varying degrees of success, suggesting that a new solder-bumping technology that combines the attributes of plating (extendibility to larger wafer and smaller bump size/pitch) with those of solder paste screening (flexibility of Pb-free alloy selection and low cost) would be viewed very favorably during this time of rapid growth for flip-chip applications.

Injection-molded solder (IMS) technology was developed at IBM Research as an outgrowth of earlier work using solder for high-performance thermal joints. In these studies it was recognized that voids in the solder interface created "hot spots" in silicon devices at the elevated power densities used during testing. Although vacuum reflow techniques could eliminate these voids, undesirable processing steps were added. Instead, a process was developed that would injection-mold solder into bi-convex-shaped preforms that could be placed at the thermal interface and reflowed in air. The crowned shape of these preforms guaranteed that wetting would start at the center and expand radially outward, thus eliminating the formation of voids at the interface [4].

Thus, it was possible with injection molding to control the flow of molten solder for a variety of interconnect applications, such as solder ball and solder column arrays as well as ceramic and organic chip carriers with 200- μm -diameter bumps. Also of interest was the ease of adaptability of injection molding to any changes in solder alloy composition, as demonstrated by its ability to process a variety of Pb-free solders with equal ease, permitting an effective comparison of 19 different Pb-free alloys [5].

The remainder of this paper is dedicated to understanding in detail the technology of IMS as it applies to wafer bumping and why it has the potential to fundamentally benefit the industry by becoming a true bumping standard. Current mainstream bumping technologies are first described, with particular emphasis on how they measure up to the important industry trends relative to IMS technology. Because lowering the unit cost of wafer bumping is a major advantage in the industry, comparisons focus particularly on this

aspect while also considering functional issues of each technology. Critical aspects of IMS development are also discussed in relationship to the industry needs mentioned previously.

Comparison of current technologies

The mainstream bumping technologies are evaporation, plating, and screening [6]. Other technologies exist, but none have had the commercial success of these three. Some of the fringe or developing bumping technologies include transfer, printing, solder jetting, and bumpless and conductive particle applications. Of these, the solder transfer type seems to have the greatest potential in the bumping industry at present.

Evaporation was the first method used for solder bumping [1], and much capacity still exists for the 200-mm wafer technology. Some of the most attractive features of this technology are that high-reliability bumps can be achieved and that it is a dry process, thus requiring relatively simple manufacturing. However, other aspects such as the consumable masks and tool cleaning play a major role in operating costs. Moreover, through-mask evaporation uses material very inefficiently, which is becoming increasingly important as recent materials requirements such as ultra-low alpha lead (LAL) and Pb-free drive have increased material costs. As the I/O count per device surpasses 3,000 and bump pitch (center to center) falls below 225 μm , yields begin to degrade with evaporation.

Within the context of the evaporation of Pb-free solders, significantly longer evaporation times [in contrast to 97Pb/3Sn (wt.%) co-evaporation] are required because of the extremely low vapor pressure of Sn, which constitutes a major proportion of the most popular Pb-free solder alloys. Yet another concern is the stability and robustness of 300-mm evaporation masks, especially at the aforementioned finer bump pitches.

Electroplated bump technology was developed to reduce many of the anticipated limitations of evaporation, specifically the issues of density and pitch. Since it is a photolithographic process, the concept of 100- μm features on 200- μm pitches or even 50- μm features on 100- μm pitches is well within technology capability. While bump technology was initiated with 200-mm silicon wafers, the process is scalable and is currently seeing fairly wide adoption with 300-mm wafers. Plating is a very integrated process—the BLM and the bump are not separable. This drives many unique chemistries and process steps (both wet and dry) for etching and cleaning because the bump metal is present during these steps, thus incurring additional cost to ensure the reliability of the bump. Relatively high operating costs are also generated by the plating materials required by this technology, since operations

are necessary to develop, procure, store, mix, analyze, and fill the tanks with plating solutions. Additionally, once acceptable operation bath life has been exceeded, a means to dispose of the large amount of chemicals is required, driving additional infrastructure costs. Size and capital cost of the plating equipment are also fairly large.

An important consideration for plating relates to the extensive activity necessary to adapt to an alternative alloy. For every new material required, new plating chemistries must be developed. Furthermore, because the process is so integrated, any plating chemistry change also affects the etching processes, so alternate chemistries may be required for those as well. If more than one alloy is to be used concurrently, it becomes necessary to either regularly swap out baths in existing platers or add new plating capacity. In the case of plating new Pb-free solder alloys, an additional significant challenge arises when the selected optimal alloy contains several components. Precise alloy composition in such multi-component alloys is critical to solder joint reliability, yet the complexity of multi-component plating baths or sequential plating systems renders such precise control difficult. Even for binary alloy compositions, the successful development of a Pb-free plating process is largely dependent upon the specific alloy selected.

Screen printing, or screening, has proven to be a viable low-cost solution for bumping both 200-mm and 300-mm wafers. While there are issues involved with the quality of screening, they are not major cost detractors, and none of the quality issues seem to be insurmountable. Screening has a lower yield than plating, but it allows parts to be reworked. A favorable attribute of screening is the ease with which different solder bump alloys can be accommodated and readily exchanged. As a result, any given Pb-free solder alloy, for example, can be directly screened in paste form, be it binary or multi-component. There are no bump-related chemistries to maintain or develop with screening and, once a supplier has obtained a qualified screening material, it is available to all users. There is wet processing in screening for the BLM as there is in plating, but a simpler BLM can be used here because a current-carrying blanket of metal is not required as in plating, which translates to a potentially lower-cost BLM for screening.

On the other hand, in that solder pastes are inherently a mixture of solder metal and flux, the subsequent reflow of solder pastes results in the formation of voids, sometimes large, in the solder joint that can adversely affect reliability. This reliability impact may be tolerated for specific low-cost applications, but must be taken into consideration if screening is to be used in high-reliability applications. The significant reduction in volume between paste form and final solid form may also impose practical limitations on the extendibility of solder printing

technology, especially for bump sizes and pitches below 75 μm on 150- μm centers. Finally, just as in the case of evaporation masks, maintaining dimensional stability of the stencil used for paste screening becomes more challenging as wafer sizes increase to 300 mm, especially at finer pitches. Employing photoresist masks in conjunction with paste deposition may alleviate the wafer size and bump pitch challenges to some degree, but not the volume reduction issue. Additionally, such photoprocessing steps will begin to have an impact on the low-cost nature of this technology.

This brief review of bumping technologies, when viewed in relationship to the current state of the industry, suggests that a gap still exists. Plating fills the high-end needs of bumping very well as long as cost pressures are absent. Screening fills the low-cost requirement but cannot meet all of the specifications required for high-end and/or high-reliability applications. A notable trend in the industry is that semiconductor costs (measured on a per-die basis) have been dropping at a faster rate than packaging costs. To keep pace, lower-cost, higher-quality bumping solutions are being sought by all manufacturers, such that the line separating “low cost” from “high end” has become very blurred. In view of these developments, IBM has recognized the need for a new C4 bumping process, especially with the advent of Pb-free solder requirements. After extensive research and development, it is believed that the injection-molded solder (IMS) technology meets the needs of such a new C4 bumping process, and the term C4NP (C4 new process) has been coined for IMS applied to wafer bumping. While sections that follow detail the essence and evolution of IMS, it is appropriate here to illustrate the relative merits of IMS that have driven the continued effort to develop IMS wafer bumping to the point of high-volume manufacturing. **Table 1**, based on data from pilot operations running within IBM, assesses IMS against the pre-existing technologies described in this section with respect to important process selection criteria.

IMS—from thermal interface to wafer bumping

Solder thermal interfaces are known to provide excellent thermal conductivity between a high-power chip and a high-efficiency heat sink. However, in IBM efforts to explore such interfaces, it became clear that any voids in the solder would produce a “hot spot” on the thermal test chip. Although vacuum reflow techniques could eliminate these, it was more desirable to produce these interfaces in air for the sake of process simplicity. Since flat solder preforms usually reflowed from the perimeter toward the center, thus causing void entrapment, changing the reflow pattern from center to perimeter was the solution. To ensure that pattern, a double-layer glass mold was produced with shallow concave cavities in the top and

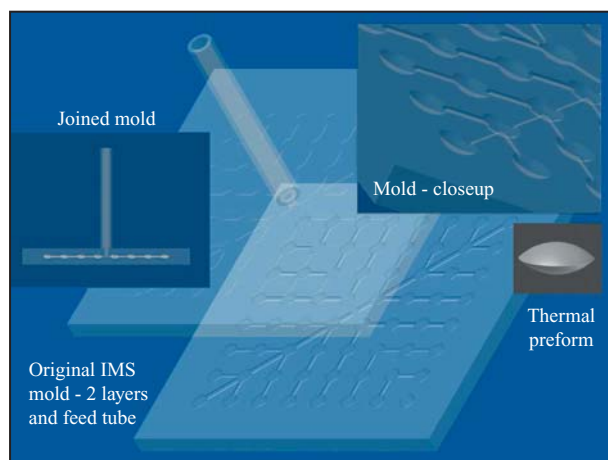


Figure 1

Solder mold for making bi-convex thermal interface preforms.

bottom mold halves. As seen in **Figure 1**, connecting sprues between the cavities and the solder feed reservoir provided the ability to supply molten solder to the cavities when the two mold halves were aligned and joined and the assembly was heated above the solder melting temperature. When the solder reservoir was pressurized, molten solder flowed through the sprues and eventually filled all of the mold cavities. Once cooled, the assembly was opened and the solder preforms were extracted, either as an array or as single preforms depending on the application. These preforms now had the exact shape of the joined concave mold cavities (bi-convex), and, when placed between a chip and a heat sink, the reflow would always begin at the central high point on both sides and expand radially outward, thus excluding any voids at the interface.

When it was recognized that the IMS method was capable of controlling molten solder in these mold geometries, it became clear that it could potentially be extended to other applications requiring solder preforms of various shapes and aspect ratios. One of the first such extensions was the high-aspect-ratio solder columns used

in ceramic column grid arrays (CCGAs). The challenge was how to provide the solder feed with such structures. Whereas previously the feed sprues were on the same level as the preforms, another method of introducing the molten solder into the deep cavities was required for these new applications. This led to the development of the first IMS head that contained a slot filled with molten solder. Such a head could be scanned over graphite molds containing the deep via holes which would form the solder columns when filled. The head also contained a clever combination of molten solder supply and vacuum which provided the ability to progressively evacuate most of the air from each successive row of via holes and maintain that vacuum until the slot with molten solder arrived to backfill the evacuated vias at ambient pressure [7]. Filled graphite molds, once cooled, would be aligned with pads containing appropriate wetting metallurgy on substrates requiring solder columns. Thereafter, the joined assembly would be heated to reflow the solder and join it to the substrate.

The preceding basic process steps would in time be applied to many other substrate applications, including ball grid arrays, interposers containing smaller (8-mil-diameter) balls, as well as individual silicon chips. In the latter case, molds would include molybdenum, stainless steel, and even polyimide sheets. It became apparent for such mold-transfer applications that the cavities for these applications should ideally be blind holes, since this would ensure that the solder could be transferred only in the direction of the substrate receiving the solder. Also, for these ever-smaller cavity sizes, the more complex vacuum IMS head could be simplified to initiate the molten solder flow simply by being pressurized above ambient, as seen in **Figure 2**.

At this point, an IBM packaging assembly group in Bromont, Canada, who, in attempting to reduce the total cost of assembly, were evaluating the low-cost wafer-bumping process using solder paste, quickly realized that pure molten solder would have inherent advantages. However, the challenge was to apply a technique for bumping individual substrates or silicon chips to bumping an entire 200-mm wafer. It first became clear

Table 1 Process selection criteria for wafer bumping.

	<i>Evaporation</i>	<i>Plating</i>	<i>Screening</i>	<i>IMS</i>
Cost	Med/high	High	Low	Low
Reliability	High	High	Low	High
Yield	Med/high	High	Med/low	High
Manufacturing flexibility	Med	Low	High	High
Engineering support	Med	High	Low	Low
Infrastructure requirements	Med	High	Low	Low
Industry proven	Yes	Yes	Yes	No

that a mold plate to cover an entire wafer could not be fabricated from the same materials used for previous smaller-area applications because of the difference in the coefficient of thermal expansion (CTE) between these materials and the silicon of the wafer. Since the transfer step required a thermal excursion from room temperature to slightly above the solder reflow temperature, then back to room temperature, the initial room-temperature alignment between mold and wafer had to be constantly maintained in order to ensure transfer and alleviate post-solidification stress. To achieve this constant alignment, mold plates having approximately the same CTE as silicon were selected for the wafer-bumping application. Silicon was initially considered as a mold plate, since various etching methods could produce the cavities which contain the solder. Cavity shape was not critical as long as the bottom of the cavity was not larger than the surface opening. Indeed, various cavities in silicon, including pyramid-shaped ones, were successfully filled and transferred. The problem with a silicon mold plate was related to another advance in IMS that was necessary for wafer-level bumping.

Early IMS fill heads typically were only 2 in. wide, with solder slots 1.5 to 1.75 in. wide. These widths allowed the filling of cavity arrays covering the range of substrate sizes then in use. However, to bump a 200-mm wafer, it was necessary to do multiple scans with these narrow heads over a much larger mold plate. Initially these scans did not overlap, leaving certain portions of the mold plates unfilled and matching areas of the wafers unbumped. When overlapping scans were tried, it became obvious that the overlap rows had inferior fill quality and that six or more scans were required for a 200-mm mold plate. The solution would require an IMS head wide enough to cover the active area of the wafer with a single scan. For such a head, it was no longer possible to use a round silicon wafer as the mold material, since the solder slots of these full-width heads would overhang the edges of the mold wafers at the beginning and end of a scan. However, at this point in the development, the fundamentals of a new wafer-bumping technology were in place, promising results superior to those for solder paste at roughly commensurate costs.

IMS for wafer bumping is, to a certain extent, a parallel process. Wafers and molds are first prepared separately, as shown in **Figure 3**. While the wafers are processed through BLM deposition and patterning processes to allow wetting of solder, the molds are filled with solder and inspected. This parallel processing reduces overall cycle time and permits each process flow to be optimized independently, thereby reducing the overall complexity of the bumping process. Only after fill quality has been deemed acceptable does a mold proceed to the subsequent

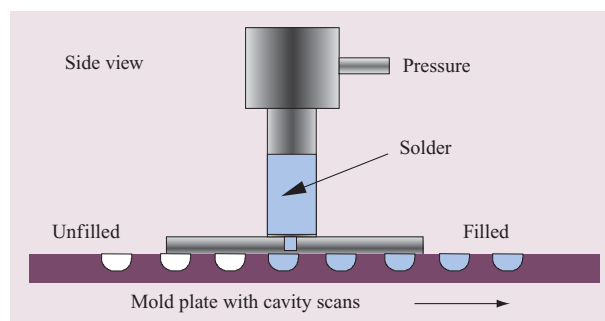


Figure 2

Basic IMS head for dispensing molten solder. Reprinted with permission from [8]; ©2004 IEEE.

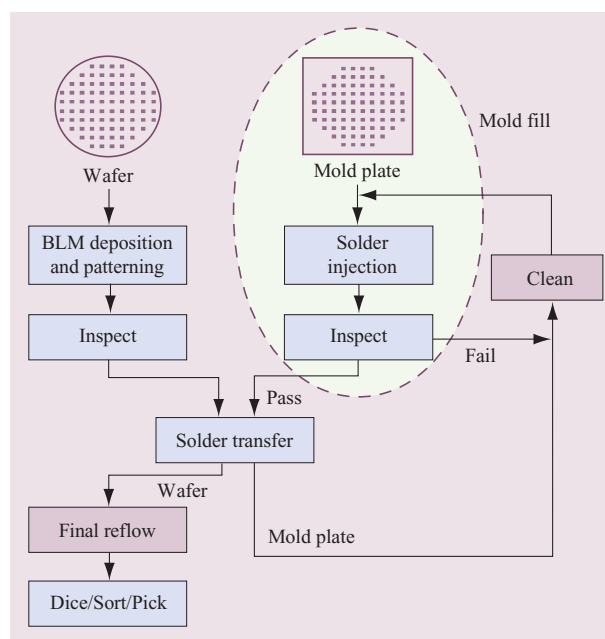


Figure 3

IMS process flow diagram. Reprinted with permission from [8]; ©2004 IEEE.

step of wafer transfer, in which contact between mold and wafer causes the transfer of solder from each filled cavity in the mold to a corresponding BLM pad on the wafer. At this stage, wafer electrical probing may be performed prior to the final step of making the solder bump fully spherical. This has the advantage that the solder preforms immediately after transfer have a wider flat “target area” of uniform height, allowing for greater probe tolerance. Once tested, wafers are reheated to reflow the solder bumps, forming uniform partially spherical shapes and

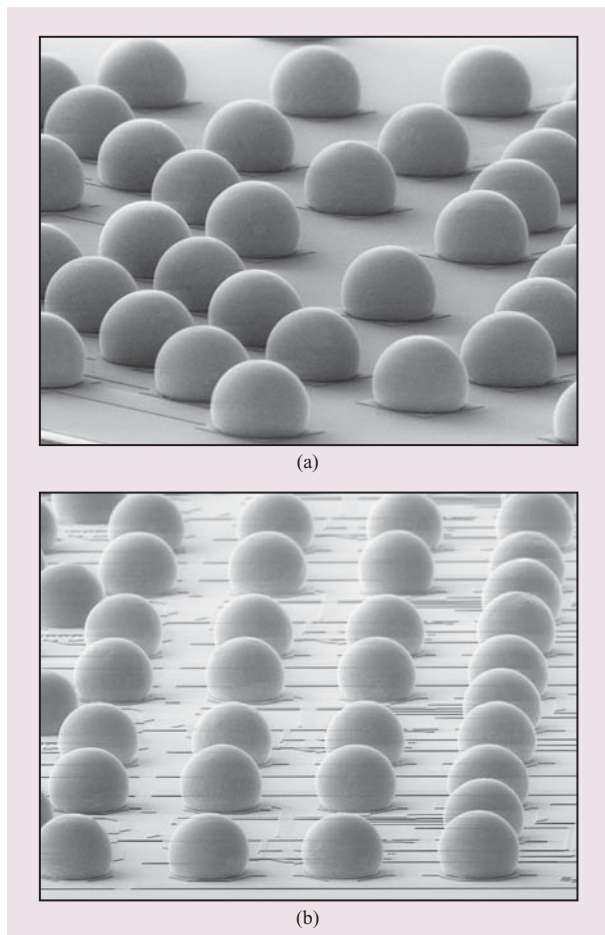


Figure 4

Lead-tin eutectic IMS bumps: (a) Diameter 4 mils; pitch 9 mils. (b) Diameter 3 mils; pitch 6 mils.

eliminating any test-probe marks that may have been left on the solder-bump surface. After reflow, standard PbSn bumps look exactly like those deposited by plating or screening, as shown in **Figure 4**.

Development of fill technology for IMS wafer bumping

The filling portion of IMS is accomplished by a stationary IMS head that uses pressure above ambient to push the molten solder from the reservoir into the solder slot and subsequently into rows of cavities in the mold plates passing sequentially beneath the head. Heads are typically wide enough to fill 300-mm molds, but may also be used for 200-mm or smaller molds. Areas of development that have been critical to the advancement of IMS wafer bumping are described in the sections that follow; they have resulted in a solder-fill process that is both manufacturable and reproducible [8].

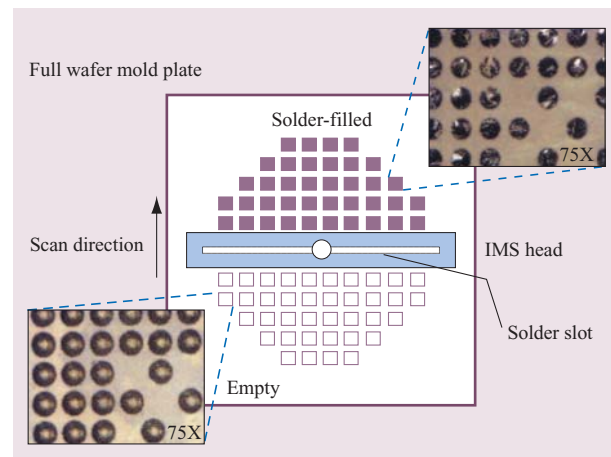


Figure 5

Top view of mold fill showing empty and solder-filled mold cavities. Each “chip pattern” is an array of cavities that matches pad array on chip.

Mold development

As IMS became focused on bumping 200-mm wafers, a reliable mold technology was required to complement the newer full-width heads that could fill the entire cavity area in one scan. The active region, in which miniature cavities are inscribed at locations corresponding to the wetting pads on the wafer, is circular; however, the mold plates must be square or rectangular in external shape such that, from beginning to end of scan, the fill head always remains on the mold plate surface, preventing the solder from leaking out because of any overhang of the solder slot over the mold edge. This is illustrated in **Figure 5** [9], which is a top view of the mold fill. Since borosilicate glass has the required CTE match to silicon and can readily be purchased in square or rectangular shapes of various sizes, this became the new standard for IMS mold plates.

Two methods of fabricating cavities proved workable and continue to be used for various applications. The first involves applying 25 to 50 μm of polyimide to the borosilicate glass surface by means of a spin-on or lamination technique. This polyimide layer is then laser-processed to produce the cavities in the polyimide layer only. Although the CTE of polyimide is quite different from that of the glass, these thin layers do not appreciably change the CTE of the composite mold from that of the borosilicate glass itself. Such composite mold plates may be produced quickly and relatively inexpensively, since a direct-laser-write machining tool does not require a mask but only location data to accurately produce the cavity arrays. However, since the polyimide layer is not as robust as the underlying glass itself, mold life is typically

less than for the second mold fabrication option. Nonetheless, for many low-volume, early-assessment or quick-turnaround-time applications, this remains a very attractive option.

The second method involves wet etching to produce the cavities directly in the glass. This option requires more processing steps but results in a mold plate that can be used for hundreds of fill and transfer operations, thus amortizing the higher mold costs to the extent that mold cost per use becomes lower than with the first polyimide method. The basic process steps for this option, as shown in **Figure 6**, are discussed in the following sections.

Mold cleaning and Cr/Cu sputtering

The first step, cleaning, is one of the most critical in mold making, along with Cu etch. The mold is first cleaned with an air gun, then with a glass cleaner and isopropyl alcohol using a clean-room cloth. The mold is then fixed on a rotary table in a mold-cleaning tool. The operation consists of mild soap vaporization, brushing, rinsing with hot, highly pressurized water, and drying. Both sides of the glass plate are cleaned. The objective is to remove any residual contaminants from glass cutting/finishing, shipping materials, and handling. After the cleaning process, dipping the glass plate in isopropyl alcohol followed by deionized water should produce a break-free film at the glass surface.

Cr/Cu films are next sputtered (physical vapor deposition) onto the glass plate. Cr is the adhesion layer and Cu the etch barrier. The Cu microstructure must be strictly controlled in order to prevent excessive etching under the metal films. Thus, the Cu film is thick, dense, and composed of large coarse grains.

Photolithography

Photolithography (steps 2 and 3) is achieved by spray-coating 24 μm of photoresist over the metallized glass plate, followed by baking in a conventional oven to evaporate solvents and enhance resist adhesion and uniformity. Two coats of photoresist are necessary to ensure a pinhole-free film. The objective of this photoresist coating is to protect the Cu film from the etching solution during the Cu etch step. The Cu layer cannot be altered at grain boundaries by the acidic Cu etching solution without jeopardizing mold final yield. When the photoresist has been exposed and developed, a final bake and UV cross-linking steps are also included.

Cu etch

Cu is spray-etched with an acidic solution. The glass plate is placed upside down in the etch tool, and the etching solution is sprayed from the bottom up, providing better solution refreshing, a higher etch rate, and optimal etch profiles. The objective of this step is to have 100% Cu

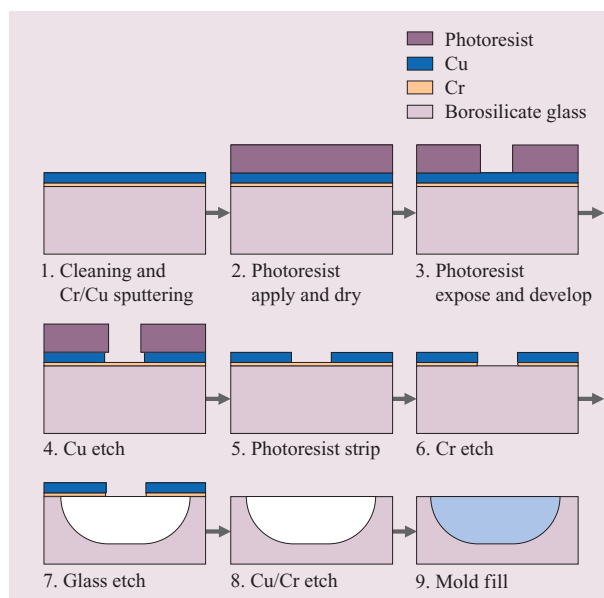


Figure 6

IMS mold manufacturing process flow.

opening yield, the straightest Cu wall, and the least amount of etch under the resist. The Cu opening diameter determines the subsequent glass etch parameters (large cavity volumes, fine pitches, etc.).

Photoresist strip

In the next step, photoresist is stripped prior to Cr etch, because the photoresist used in our development work is not compatible with the Cr etching solution.

Cr etch

As with Cu, Cr is also spray-etched with a standard potassium permanganate solution. The same equipment is utilized for the Cu/Cr etch steps, and molds are processed in the same manner.

Glass etch

The main step, glass etch, is performed with a heated dilute hydrofluoric acid (HF) solution. The etch is accomplished using an immersion process, the glass plates being immersed in the solution and placed horizontally (cavity side down) in the tank. The tank has a laminar flow, cascading on four sides. The laminar flow and cascade provide effective refreshing of the solution at the glass surface. The HF works isotropically, giving the etch cavity a small barrel shape, with a bottom flat reflecting the original Cu opening diameter. To achieve consistent etching, proper chemical control of the HF etching solution is imperative.

Table 2 Mold yield—qualification.

<i>IMS mold</i>	<i>Yield chip sites (%)</i>	<i>Pinholes (%)</i>	<i>Cracks (%)</i>	<i>Contaminations (%)</i>	<i>Wormholes (%)</i>	<i>Bridges (%)</i>	<i>Missing cavities (%)</i>
Average	96.6	2.0	0.2	0.2	0.2	0.9	0.8
451A	98.2	1.0	0.0	0.5	0.3	1.1	0.0
451B	98.2	1.3	0.0	0.3	0.3	0.8	0.0
451C	97.4	1.3	0.0	0.8	0.0	0.5	0.5
452A	98.4	0.8	0.0	0.3	0.0	0.3	0.5
452B	91.2	0.5	0.5	0.0	0.0	0.8	7.8
452C	96.6	1.6	0.0	0.0	0.0	0.3	1.8
453A	91.2	1.0	1.3	0.5	0.0	0.8	6.0
453B	99.5	0.0	0.0	0.3	0.0	0.0	0.3
453C	97.7	1.0	0.0	0.0	0.3	0.3	1.0
454A	92.5	7.0	0.3	0.0	0.2	1.6	0.0
454B	98.4	0.8	0.0	0.3	0.5	0.8	0.0
454C	91.5	5.4	1.3	0.5	0.5	3.9	0.8
455A	98.7	1.0	0.3	0.0	0.0	0.5	0.0
455B	96.4	2.8	0.3	0.5	0.0	0.5	0.0
455C	94.6	5.4	0.0	0.0	0.0	1.1	0.0
456A	97.9	1.8	0.0	0.3	0.0	0.8	0.0
456B	98.7	0.3	0.5	0.3	0.3	1.1	0.0
456C	98.7	1.0	0.3	0.0	0.0	1.1	0.0
457A	96.9	1.8	0.3	0.0	0.3	0.5	0.8
457B	97.9	1.0	0.0	0.3	0.8	0.5	0.0
457C	96.6	2.1	0.3	0.5	0.5	0.8	0.0
458A	94.5	5.2	0.0	0.0	0.3	1.6	0.0
458B	99.5	0.3	0.0	0.3	0.0	0.3	0.0
458C	96.6	3.1	0.3	0.0	0.0	1.6	0.0

Cu/Cr removal

As the last step, once the cavities are etched, Cu/Cr films can be removed using the same solution and equipment as in steps 4 and 6. The mold is now ready for inspection and the actual solder filling.

Wet process summary

Developing the wet process had its share of challenges. For example, solutions had to be found for mold camber and small or missing cavities. Yield optimization was required for glass cleaning prior to sputtering. Finally, optimal Cr/Cu film deposition parameters had to be determined, and the resist process had to be improved.

Manufacturing data

To determine that the mold-making process is robust and capable of producing molds with repetitive and uniform cavity shape and volume, a qualification run was initiated and manufacturing data was collected.

For the qualification the following method was applied: 24 glass molds were built (eight lots of three molds), sputtered on eight different days, from two different incoming glass lots. The test vehicle used was a 200-mm wafer pattern, 60.9 mm² per chip (6.89 mm × 8.84 mm), 386 chips per wafer, 401 C4s per chip (154,786 C4s per wafer). The pass/fail criteria were a minimum 95% yield for all defects (chip yield), a maximum 2% critical defect¹

¹A critical defect is a defect affecting wafer final yield.

Table 3 (a) Cavity measurements; (b) cavity measurements/five locations per mold.

	<i>Top diameter average</i> (μm)	<i>Top diameter sigma</i> (μm)	<i>Bottom diameter average</i> (μm)	<i>Bottom diameter sigma</i> (μm)	<i>Depth average</i> (μm)	<i>Depth sigma</i> (μm)	<i>Volume average</i> ($\times 10^4 \mu\text{m}^3$)	<i>Volume sigma</i> ($\times 10^4 \mu\text{m}^3$)	<i>Accept ratio</i> (top diameter/depth)
(a)									
Molds	154.9	3.2	32.0	2.5	60.8	0.6	75.0	3.8	2.6
Molds/fill	153.9	2.9	32.6	2.2	61.2	0.5	77.7	3.4	2.5
(b)									
Location									
J2	153.7	1.4	31.2	1.2	60.7	0.2	76.7	1.5	2.5
A14	157.5	1.1	33.2	1.3	61.3	0.1	81.5	1.2	2.6
J14	154.4	1.1	31.7	1.1	60.7	0.1	77.4	1.1	2.5
S14	157.0	1.1	33.9	1.2	60.8	0.1	80.5	1.2	2.6
J28	152.0	1.2	30.2	1.3	60.3	0.2	74.5	1.2	2.5

Table 4 (a) Cavity measurements; (b) cavity measurements/five locations per mold.

	<i>Top diameter average</i> (μm)	<i>Top diameter sigma</i> (μm)	<i>Bottom diameter average</i> (μm)	<i>Bottom diameter sigma</i> (μm)	<i>Depth average</i> (μm)	<i>Depth sigma</i> (μm)	<i>Volume average</i> ($\times 10^4 \mu\text{m}^3$)	<i>Volume sigma</i> ($\times 10^4 \mu\text{m}^3$)
(a)								
Molds	158.5	3.2	39.4	2.4	57.0	0.7	77.5	3.6
(b)								
Location								
J2	159.0	1.7	40.0	1.6	56.9	0.2	77.8	1.8
A14	158.6	1.8	39.5	1.5	56.9	0.2	77.4	1.8
J14	157.0	1.7	39.2	1.4	56.7	0.1	76.4	1.7
S14	159.0	1.7	39.1	1.5	57.1	0.2	78.0	1.8
J28	159.0	1.6	39.3	1.5	57.2	0.2	78.1	1.7

(chip yield), and having cavity volume meet the bump volume specifications. The results obtained are summarized in **Tables 2** and **3**. The minimum 95% yield for all defects was met, and a 96.6% chip yield was obtained. The critical defects (bridges and missing cavities) yielded at 1.7% for a targeted maximum of 2%. The volume of mold cavities calculated from the measured cavity dimensions met wafer bump volume uniformity specifications ($55\text{--}115 \times 10^4 \mu\text{m}^3$). The cavity aspect ratio (top diameter/depth) is less than 2.8, as

required to produce optimal fill characteristics. In Table 3(b) the objective is to identify the volume distribution across the mold and its repeatability.

Following the qualification, pilot line simulations were run over time; results are summarized in **Table 4** and **Figure 7**. As shown in the figure, a perfect mold yield was achieved by the end of 2003. As for the qualification, mold cavity volumes met wafer bump volume specification and are repeatable across the entire mold.

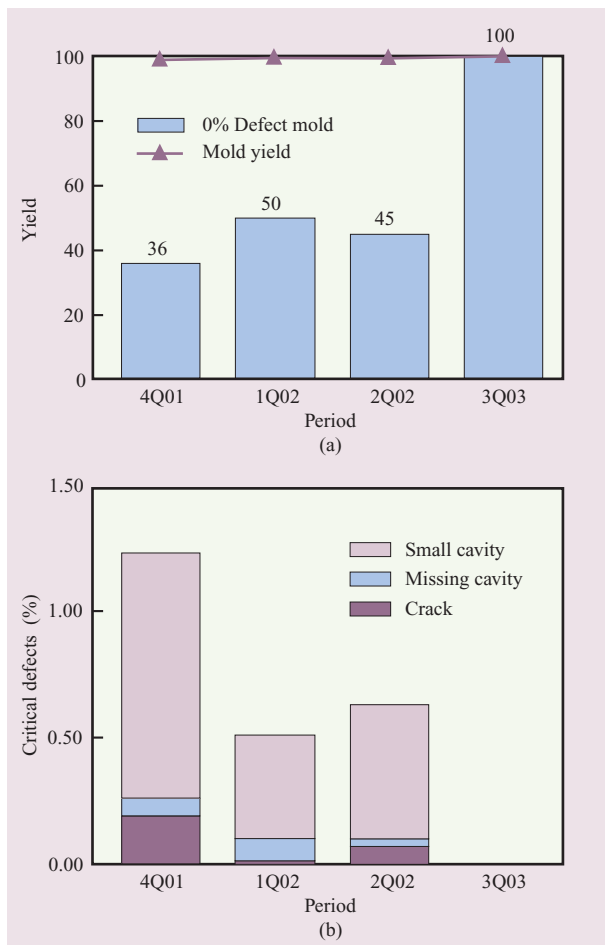


Figure 7

(a) Glass mold yield (chip sites) and (b) glass critical defects during line simulation.

The mold-making method described above has met all of the requirements of the next operation, mold fill and transfer. The mold covers the entire wafer, has a smooth, flat, transparent surface, and is CTE-matched to the wafer. It is also rectangular, with cavities inscribed in the wafer region; cavity volume and shape are repeatable and meet specifications, as shown in **Figure 8**.

Head development

As mold plate development continued toward meeting the requirements of manufacturing, head development had to keep pace. As previously noted, earlier heads were only 2 in. wide. They were fabricated from rigid materials such as thick glass or metal with a flat bottom that maintained a sliding solder seal with respect to the top surface of the mold. When molds for CGAs were graphite plates, these rigid IMS heads were perfectly acceptable, since the natural lubricity of the graphite ensured that the head

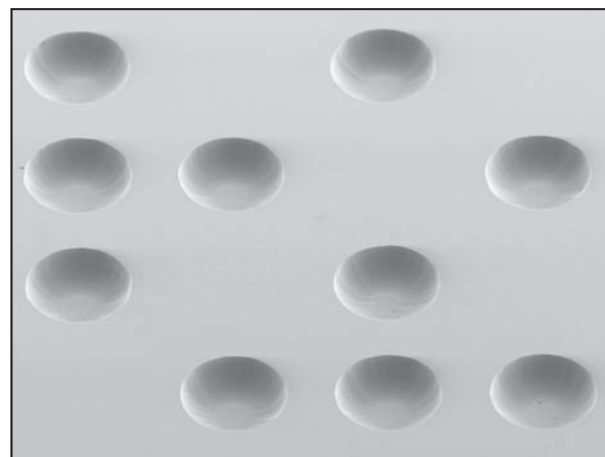


Figure 8

IMS mold.

could scan smoothly over the top surface of the mold and efficiently fill the via holes. As mold materials evolved for wafer-bumping applications, it became necessary to coat the bottom of the IMS heads with materials having low friction coefficients.

A fundamental principle of IMS is the need to provide a solder seal such that the molten solder under pressure can easily flow into the mold cavities as the head is scanned without leaking beyond the solder slot area at the bottom of the head. Unlike solder paste, which has a very high viscosity, the viscosity of molten solder is only two centipoise, or twice that of water. Consequently, micron-scale seal defects produce small leaks that can cause solder bridges between adjacent filled solder cavities (which can potentially produce solder shorts on the wafer when transferred), while mil-scale seal defects can purge a solder reservoir in seconds, leaving a large puddle of molten solder. At the same time, the seal must not be so tight that the air in the mold cavities cannot leak out at the mold-head interface, since this would prevent the solder from entering the cavities.

This pressure balance between preventing solder leakage and allowing air leakage is at the heart of the IMS head and process. Such a balance could be achieved for the 2-in.-wide heads by selecting coatings with a slight compliance while maintaining good control of both mold-head co-planarity and joining pressure. However, maintaining the pressure balance became more challenging as the width of the head grew from 2 in. to 8 in. (200 mm) and later to 12 in. (300 mm). At such widths, two options exist to achieve the critical sliding solder seal: 1) accommodate the existing shape (i.e., not perfectly flat) of the larger full wafer mold plates with a head that contains a flexible fill blade, or 2) force the

mold plates to be flat under the head by using a very rigid head with a more compliant seal mechanism. Both of these options have successfully filled mold plates with 200-mm widths, while the latter option has been favored more recently for fill of 300-mm mold plates, achieving excellent fill results. Of course, controlling initial mold flatness in this option is important in order to avoid the need for excessive head force.

Solidification development

As the application of IMS broadened to include Pb-free and 300-mm wafer bumping, a subtle but important process change in the mold fill process was implemented. This change involves the state of the solder immediately after it is dispensed into the mold cavities. Whereas previously the solder remained molten as it exited behind the fill head, the new process, produced by a precise combination of head and mold plate temperatures, ensures solidification of the solder immediately after deposition in the mold cavities; hence, prior to exiting the fill-head region. This has three very important advantages.

First, molten solder is susceptible to surface tension effects caused by the trailing edge of the fill head. Such effects would at times produce “streaking” of the molten solder—small molten solder deposits left on the mold surface instead of in the mold cavities, which could bridge between two filled cavities and cause problems during the subsequent transfer step. Transfer assumes intimate contact between the mold plate surface and the wafer, and these solidified streaking deposits interfere with such a configuration. The resultant gap provides a path for bridging between two bumped wafer pads that can cause electrical problems. Solidifying the solder underneath the head avoids streaking, and hence bridging.

The second advantage relates to the fact that unrestrained molten solder tends to assume its lowest-surface-energy form—a sphere. Once solidified, these “balled-up” solder preforms would be relatively “loose” in their cavities and subject to inadvertent removal during pre-transfer handling of the molds. Originally, such “balling up” was reduced by maintaining a certain level of oxygen in the fill area in order to overcome the natural surface tension effects by slightly oxidizing the solder. However, these oxygen levels would leave excessive oxide residues on the fill head and mold surfaces. Ensuring that solidification occurs under the restraining head surface causes the solder to remain flat and well adhered to its cavity without the need for oxygen, thus reducing oxide formation, which in turn reduces the frequencies of fill-head maintenance and mold-plate cleaning.

The third benefit of solidification is that the solder volume uniformity is equal to the volume uniformity of

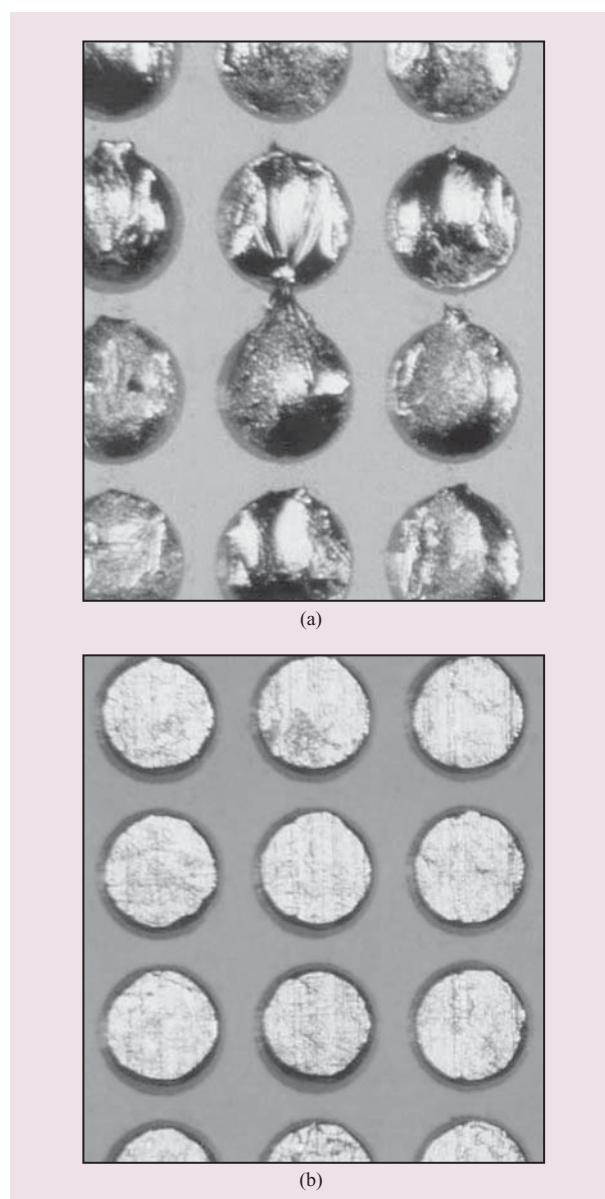


Figure 9

(a) No solidification; solder bridge. (b) Solidification. Reprinted with permission from [8]; ©2004 IEEE.

the mold cavities themselves. Since cavities are fabricated photolithographically, their volume uniformity is extremely good. As can be seen in comparing **Figures 9(a)** and **9(b)**, filled cavities with solidification have the top of the solder exactly coplanar with the top surface of the mold plate. Previously, the filled cavities could vary in volume based on how much of a “solder crown” there was above the mold plate top surface. This optimized solder volume precision translates directly into bumps of extremely uniform volumes and thus heights.

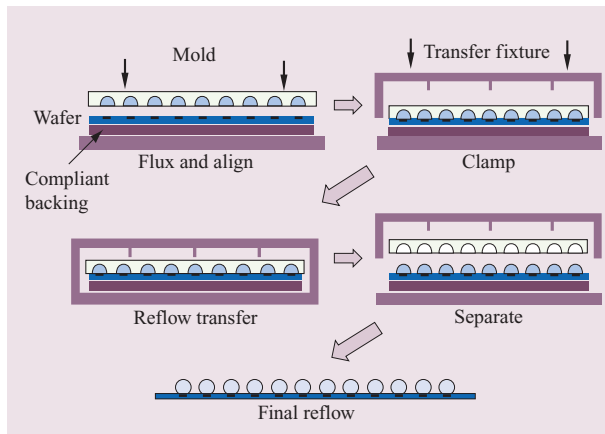


Figure 10

Mold-to-wafer transfer sequence.

Filled mold inspection development

The mainstream bumping techniques described previously apply the solder material directly to the wafer, be it evaporated, plated, or in paste form. If there are any problems with the application process, this translates to a yield hit on the wafer that cannot easily be eliminated. On the other hand, IMS is a transfer process in which the application of the molten solder from the IMS head is not directly on the wafer but rather on the mold plate. Therefore, the molds can be inspected after the fill step to determine whether there are any cavities that are only partially filled with solder or missing solder altogether. Because of the solidification improvement just described, the fill step is typically very robust. Nonetheless, the inspection of filled molds provides another safeguard to prevent bump yield problems on the wafer, provided that it can be done in a cost-effective manner. For this reason, efforts were dedicated to the development of an effective automated approach to inspection of filled molds.

The first critical area of development concerned the definition of a fill defect. While a “missing fill” is self-evident, definition of a partial fill required understanding the relationship between acceptable solder bump volume and cavity shape in order to make insufficient volumes detectable by an automated inspection. Methods to ensure adequate contrast between the solder and mold surfaces was a second area of activity. A third key factor, more related to manufacturing costs, was determination of the appropriate cutoff conditions for disposition of the filled mold. Both missing and partial fills can be reworked, but each incurs separate incremental costs; thus, maximum defect levels were calculated for the specific mold rework that would be recommended. At defect levels beyond these cutoffs, the more cost-effective disposition would be to have the molds emptied of their

solder content, and thereafter prepared for refill. While such a fill condition would indicate that the fill process has deviated significantly from its routine parameters, and would be a rare occurrence, a cost-effective mold inspection approach ensures that fill problems are not only quickly highlighted but also readily isolated at the mold level without affecting the wafers.

Development of the IMS mold-to-wafer transfer process

Once molds are filled and inspected, the next and final step of wafer bumping using IMS is the transfer process. Only at this step does the IMS process involve the actual wafer. Transfer involves a mechanical joining of the top surfaces of both mold plate and wafer in a mirror-image fashion. The basic sequence of transfer is shown in **Figure 10**. The following paragraphs discuss critical aspects of each individual step together with the areas of development undertaken to address these aspects.

As a first step, the mold and/or wafer is coated with a thin layer of flux to reduce the solder oxide to enable solder wetting of the BLM during the subsequent reflow temperature excursion. Flux selection, viscosity, distribution, and thickness became increasingly important areas of development when evolving to the 300-mm wafer size. The main challenge was to strike a balance between ensuring flux presence on all bump sites across this large span without creating regions of excess flux that might otherwise prevent contact between bump and BLM.

The wafer is then placed in a transfer fixture, and the mold is placed over the wafer in a roughly aligned fashion. The wafer and mold may then be precisely aligned by moving the mold in reference to the stationary wafer. Because of the transparency of the borosilicate glass mold plate, the alignment may be accomplished by direct line-of-sight of specific filled-cavity locations on the mold with respect to corresponding pad (BLM) locations on the wafer. By aligning three such locations at appropriately separated points of the mold, global alignment of all cavity/pad pairs is achieved. A critical area of development for this step resided in fixture design to allow precise relative alignment without disturbing the sensitive distribution of the previously applied flux layer.

Once globally aligned, the assembly is clamped by closing the cover of the fixture in such a way that contact points behind the mold begin to provide uniform pressure over the mold–wafer interface. During initial work with relatively small substrates/wafer portions, mold surface coplanarity, both locally and globally, did not appear to have any repercussions for bump-pad contact. This was not the case for full wafer sizes. Owing to the relative flexibility of these large, thin slices of silicon, a compliant coating on the fixture base was devised to allow overcompression such that the wafer could “track” any

slight mold-plate curvatures. Holding-pin mechanisms were designed such that intimate mold-face-to-wafer-face contact across the full wafer span could be ensured during the reflow step without creating localized pressure points that would risk damage to either mold or wafer.

The assembly is then placed in a reflow furnace with a temperature profile selected to provide a temperature above the solder melting point for the desired amount of time. This causes the solder in the cavities to melt and surface tension of the flux-cleaned alloy forces the molten solder volume against the BLMs, producing a metallurgical bond. For each alloy, profiles were developed that ensured wetting while avoiding excess turbulence of the liquid solder within the restricted cavity region. As the assembly is cooled, the solder volumes in the cavities again solidify but are now strongly bonded to the wafer and only weakly attached to the cavity walls.

Following reflow, the transfer fixture is unclamped and the mold is lifted away from the wafer. This was initially accomplished by applying a vacuum to the underside of the wafer while simultaneously applying a vertical force using lifting pins against areas of the mold outside the wafer. While acceptable for lower-bump-density applications, the forces necessary for higher bump populations induced bending moments that could cause shearing effects on the bump-pad interface. To avert this, a gasketed fixture was developed that uses pressurized air or nitrogen both to initiate separation and to effect the final lifting of the mold. This particular means of applying pressure was also found to be more easily “tunable” to the actual density of the wafer-bumping application.

At this point, the wafer, having cavity-shaped solder bumps, may be fluxed again and sent for a final reflow to make the solder bumps spherical. Because the solder bump is already homogeneous in composition, this final reflow may or may not be necessary depending upon the particular application. The cavity-shaped bumps have the added advantages of 1) being extremely consistent in height across the entire wafer and 2) having a flattened top surface that may be more amenable to probing for final wafer test.

Evaluation of the IMS wafer-bumping process

Those characteristics that distinguish the molded solder-transfer process of IMS from other solder-deposition processes warrant verification as to whether the “fill-then-transfer” process produces robust solder bumps. This section reviews data obtained so far that supports the compatibility of IMS with current solder-bump requirements.

BLM (UBM) compatibility

To prepare for the IMS solder transfer process, wafers are processed with a BLM/UBM pattern which mirror-

Table 5 Results of mechanical and reliability testing for flip-chip on laminate BGA using IMS bumped chips on Ni(P) BLM. From [9], reprinted with permission.

<i>Test description</i>	<i>Results</i>
T0 chip tensile pull (g/bump)	71.5 avg 62.3 min
T0 bump shear (g/bump)	
• Shear height in BLM	71.5 avg 52.8 min
• Shear height in solder	37.3 avg 33.2 min
HAST 130°C/85% RH/3.6 V/96 hr	0/15 fail
THB 85°C/85% RH/3.6 V/1,000 hr	0/15 fail
HTS 150°C/2,500 hr	0/15 fail
ATC -40°C/125°C/1.5 cph/1,000 cycles	0/15 fail

HAST: Highly Accelerated Stress Test; THB: temperature/humidity bias; HTS: high-temperature storage; ATC: accelerated thermal cycling; cph: cycles per hour.

images the solder-filled cavities of the glass mold. The BLM (ball-limiting metallurgy) serves both as a wettable surface for the transferred molten solder and to confine the lateral flow to the pad area. In this way, IMS is similar to other bumping processes that apply the solder after the BLM deposition and patterning on the wafer, and different from plating, which applies the BLM as an integral part of the solder-bump deposition process.

Several commonly used methods have been developed to fabricate BLMs. One such method, electroless Ni(P) plating, has been a popular choice for low-cost stencil paste screening manufacturers because its simple processing steps do not require photomask processing. To facilitate electroless Ni(P) plating on an Al terminal pad, a single or double zincate process has been developed [10]. Through pre-cleaning followed by activation, the Al oxide layer is removed, and a thin layer of Zn is applied. During the electroless Ni(P) plating stage, Zn is replaced with Ni, forming a strong bond between the Ni and Al. The process is similar for a Cu terminal pad except that the surface is first cleaned with diluted etchant and then activated with a Pd solution, after which the Ni(P) film [10, 11] can be plated to the desired thickness. All of these etch, seed, zincate, and Ni(P) plating solutions are commercially available at low cost [12]. The combination of low-cost IMS bumping with such a low-cost BLM represents an attractive solution for cost-sensitive applications [8]. For this reason, evaluations of the ability of IMS to deposit solder bumps on plated Ni(P) BLMs were undertaken. In this case, eutectic solder was used for the bump. **Table 5** summarizes the description and results of this evaluation.

Another relatively low-cost BLM involves a sequence of processes that include blanket deposition of the BLM



Figure 11

SnCu Pb-free IMS bump as joined to Cu BLM.

layers onto the wafer surface,² application of photoresist, and exposure/development of an input/output dot pattern in the resist, followed by subtractive etching of the BLM layers not covered by photoresist. After photoresist stripping and cleaning, a thin layer of flux is applied to either the wafer or mold plate surface. Thereafter, the solder-filled mold plate with the mirror-image pattern is aligned and transferred to the BLM pattern on the wafer. Compatibility of this type of BLM with IMS was also successfully assessed, again with eutectic solder, with major reliability results shown in **Table 6**.

Pb-free compatibility

The particularities of Pb-free solder are driving adaptation and development of other BLMs. Since these solders normally have high Sn content, such as 96.3Sn3.7Ag and 99.3Sn0.7Cu, they are consequently highly reactive with Cu. One means to address this is by the use of a thick electroplated Cu layer in the BLM. **Figure 11** is a cross-sectional view of the as-joined structure. Cu–Sn intermetallics (IMCs), both Cu_6Sn_5 with the scallop shape and Cu_3Sn , more planar, are formed at the solder–BLM interface, which helps to form a strong solder joint. Reliability data for Sn–Cu Pb-free alloy on thick Cu BLM is shown in **Table 7**.

As with any flip-chip package, it is important to provide the appropriate complementary UBM for a chosen solder alloy. Reliability data for Pb-free IMS-bumped wafers is not as dependent on the IMS transfer process as it is on the selected Pb-free solders and UBM structure. Typical Pb-free solders have higher melting temperatures and higher yield strength than eutectic PbSn

Table 6 Test of (a) 14.2-mm chip on 42.5-mm laminate BGA (SLC); (b) 18.5-mm chip on 42.5-mm laminate BGA (HyperBGA). From [8], reprinted with permission; © 2004 IEEE.

<i>Test description</i>	<i>Results</i>
(a)	
JL4 + HAST 110°C/85% RH/3.7 V/264 hr	0/48 fail
JL4 + DTC –40°C/115°C/2,000 cycles	0/42 fail
JL4 + ATC 0/125°C/3,000 cycles	0/41 fail
JL4 + HTS 150°C/2,000 hr	0/43 fail
JL3 + HAST 130°C/85% RH/no bias/96 hr	0/23
JL3 + DTC –55°C/125°C/1,000 cycles	0/39
(b)	
JL4 + HAST 130°C/85% RH/3.7 V/96 hr	0/15 fail
JL4 + DTC –40°C/125°C/1,000 cycles	0/72 fail

SLC: surface laminar circuit; DTC: deep thermal cycling.

Table 7 Test of 14.2-mm chip on 42.5-mm laminate BGA (SLC).

<i>Test description</i>	<i>Results</i>
JL3 + HAST 130°C/85% RH/No V/96 hr	0/48 fail
JL3 + DTC –55°C/125°C/1,000 cycles	0/40 fail

alloy. Their thermomechanical fatigue behavior is quite different from that of the binary PbSn alloy.

An alternative means of addressing the Cu consumption issue is the use of Ni either as a replacement for, or in conjunction with, a Cu layer. Be it electroless plated Ni(P), as previously described, electrolytic plated or sputtered Ni(V) [11, 13, 14], the Ni has been shown to react significantly more slowly than Cu with these high Sn contents. In all cases, IMS-transferred Pb-free solder bumps have demonstrated excellent metallurgical bonding to the Ni BLM metallurgies.

Solder-joint strength of IMS-transferred Pb-free bumps was also an important factor. To evaluate this effect, bump shear tests were performed on wafer bumps deposited by the IMS process using both SnCu and SnAgCu Pb-free solders and compared with plated bumps. All bumps in this evaluation used thick Cu BLM pads patterned and plated on the chip. As shown in **Figure 12**, the shear strengths for IMS bumps were equivalent to those for the plated bumps. The higher shear strengths of the SnAgCu bumps are due primarily to the higher yield strength and hardness of this alloy compared with those of the Sn0.7Cu alloy.

²Ta, TiW, Cr, or Ti are commonly used metals for the adhesion layer to the wafer passivation, while Ni and/or Cu are used as diffusion barrier and wettable layers.

IMS and Pb-free alloys—A new low-cost process for a new C4

As has already been noted, evaporation is considerably less feasible for typical Pb-free alloys because of the low vapor pressure of Sn, the main component. Plating has been able to transition to some Pb-free alloys, but plating multi-component alloys is very challenging and costly. Solder pastes are formulated for Pb-free alloys in the same manner as for SnPb eutectic, with fluxes optimized for each alloy. However, any solder paste process, whether eutectic or Pb-free, suffers from fundamental limitations: voiding and difficulty in scaling to finer bump size and pitch. Considering the focus on environmental elimination of lead for all electronic packaging, the timing is opportune for a new wafer-bumping technology that more specifically addresses the needs of Pb-free processing without impeding industry momentum in the areas of lower costs and higher density. On the basis of the previously described compatibility assessments of IMS for Pb-free alloys coupled with advantages inherent in its process, IMS is considered to be such a technology. The principal advantages of IMS are the following:

- Alloy flexibility which includes ternary and quaternary or higher component alloys.
- No material volume change from deposition to final bump, providing extendibility to very fine bump size and pitch.
- Low material costs due to simple bulk solder form factors instead of requirements for conversion to pastes, preforms, or chemical solutions.
- Efficient solder usage, providing environmental and economic benefits.
- Process simplicity similar to that of stencil printing.

A brief review of each of these advantages follows.

While the industry continues to grapple with the selection of the ideal Pb-free “drop-in” replacement for PbSn eutectic, IMS has been selected as the process of choice to compare the basic metallurgical properties of 19 different Pb-free alloys [5].

The alloy independence of IMS is straightforward—to use a Pb-free alloy of a desired composition, a solder vendor simply prepares the alloy by combining the component metals in their desired weight percentages. The resulting alloy can be made in any form factor compatible with supplying the IMS head reservoir. Typically, solder shot is one of the lowest-priced form factors and is ideal for automated resupply of the IMS head reservoir.

Because IMS uses pure alloys throughout the entire process, the only change the solder undergoes is from solid to molten state and back to solid state. Pure solder alloy is deposited in the cavities of the mold plates, with

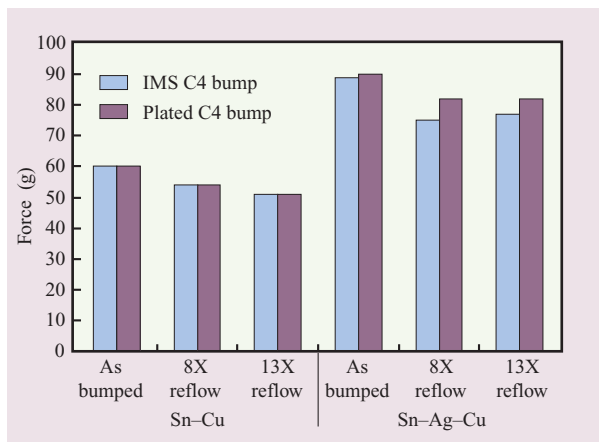


Figure 12

C4 shear strength comparison: IMS-transferred vs. plated bumps.

no volume reduction from deposition to final solder bump. As such, IMS can be used for smaller bump sizes and tighter pitches than is possible with paste, because the latter incurs solder volume reductions of as much as 50%.

Since IMS uses bulk solder alloys in their lowest-cost form factors and melts these to process pure molten alloy, all material conversion issues are avoided. There is no requirement to produce or treat multiple chemical solutions, as is required for plating. There is no requirement to produce homogeneous mixtures of flux and fine solder particles, as is the case for solder screening. Again compared with solder screening, there is no requirement to control solder particle sizes in order to meet demands of fine pitch deposition. The lack of these requirements implies a raw material that is not only less expensive but also more environmentally friendly.

IMS uses one bump-pattern-defining layer, the mold plate, to transfer bumps to hundreds of wafers; only the solder volumes required for each bump exist in the mold plate prior to transfer. Thus, no solder waste occurs in IMS Pb-free wafer bumping. Evaporation is notoriously inefficient in its use of deposited materials, with material waste of more than 98%. Even for plating, subtractive etching in the presence of the solder bump also removes some of the plated solder, since it is the solder that acts as the mask when the seed layer is being etched. While Pb-free solders may be considered more environmentally acceptable than those containing Pb, it is nonetheless desirable to use these new materials in the most efficient manner possible.

Finally, although IMS exhibits the aforementioned strengths, it does so with a manufacturing process that is

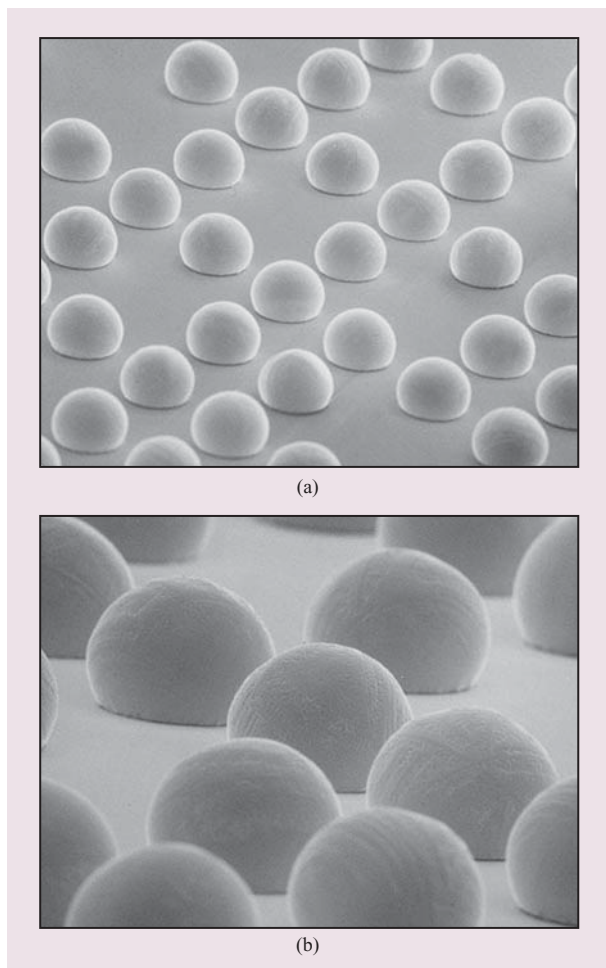


Figure 13

SnCu bumps: (a) 70X; (b) 200X.

not very different from simple solder stencil printing. With IMS, the “printed” material is pure molten alloy, and the “stencil” is a solder-mold plate. While it is true that IMS employs a transfer step that is not required for stencil printing, this can be viewed as an additional benefit, since inspection done prior to transfer ensures that valuable silicon surface area is bumped with only 100% yielded molds. Again, as is true of PbSn eutectic bumping, Pb-free bumps produced by IMS look identical to those produced either by plating or by stencil printing [Figures 13(a) and 13(b)].

Manufacturability evaluation of Pb-Free IMS

Important properties of the most prevalent leaded and lead-free solders are compared in **Table 8**. It can be seen that the Pb-free solders in general have higher yield strengths than does the leaded solder. This is partially attributed to the higher Sn (or lack of Pb) in such solders,

Table 8 Properties of solder alloys [15, 16].

	Pb-3Sn	Sn-37Pb	Sn-0.7Cu	Sn-3.5Ag
Melting temp. (°C)	315–321	183	227	221
Elastic modulus (GPa)	9.5	29	—	37
Yield strength (MPa)	5.8	16.1	21.4	33.9
Tensile strength (MPa)	9.8	31–46	31	55

Table 9 Eutectic PbSn bump data. From [8], reprinted with permission; © 2004 IEEE.

Wafer size (mm)	200
Chip size (mm)	10 × 10
Bumps per chip	401
Bumps per wafer	154,786
Bump pattern	Array
Bump pitch (mils)	4 on 9
Bump heights (μm)	
• Wafer mean	92.2
• Wafer sigma	2.8
• Chip sigma	1.8

as can be seen by comparing the properties of a 63Sn37Pb eutectic alloy with those of the 3Sn97Pb solder. The presence of Ag in certain Pb-free alloys can also significantly affect the mechanical properties, as can be seen by comparing the Sn-3.5Ag alloy with the Sn-0.7Cu alloy. These property differences were important considerations when the IMS process was transitioning from leaded to Pb-free solders. The principal adaptations from a manufacturability point of view are discussed in the paragraphs that follow.

One key requirement for confirming the extendibility of IMS for Pb-free wafer bumping is to track the encouraging results achieved for eutectic bumping that have previously been reported [5]. For example, it is useful to compare the solder volume uniformity of eutectic and Pb-free alloys. As is true of other bumping processes, it should be noted that bump height uniformity with IMS is dependent on the uniformity of the mold cavity and of the BLM diameter. It is assumed that good control of BLM diameters is provided for both eutectic PbSn and Pb-free BLM metallurgies. A preliminary manufacturing line qualification using 36 wafers produced the eutectic bump data shown in **Table 9**. For these 1-cm-square chips, chip yield was 99.2%, and bump yield was greater than 99.995%. At present, 0.5% of chip yield losses are due to the transfer process, as indicated by a comparison of mold fill and wafer chip yields. All data represents work done on 200-mm wafers, with extensions to 300-mm wafers expected to be straightforward on the basis of early manufacturing trials.

Further 200-mm designs are currently in evaluation, including a 100-μm feature on a 250-μm pitch with more

than 200,000 bumps per wafer and a 100- μm feature on a 200- μm pitch with more than 300,000 bumps per wafer. For 300-mm wafers, bump quantities will increase to 750,000 and, shortly, more than a million bumps per wafer!

As can be seen from **Table 10**, bump uniformity data from two early lots of three and six Pb-free 200-mm wafers, each containing 14.7-mm-square chips, compares very favorably with the eutectic data. Thus, the basic aspects of IMS remain consistent between eutectic PbSn and Pb-free alloys. However, lower chip yields were encountered at the early stage; since this was partially related to the larger die size, further manufacturing development work has been required to optimize solder dispensing at higher processing temperatures while accommodating the molten solder characteristics of tin-rich Pb-free alloys.

For the low-cost nature of the IMS process to be realized in manufacturing, it is necessary to confirm the reuse of the mold plates. With a reuse number of several hundred, mold-plate costs per wafer are negligible. Two sets of data confirm that this is a reasonable expectation. In pilot-line runs, mold plates have been used (i.e., subjected to actual fill, transfer, and cleaning steps) more than 60 times. Comparing yields of the most recent runs with those of the initial runs revealed no difference in mold-plate quality. Another experiment to validate mold robustness was to simulate processing in a laboratory setting by subjecting mold plates to more than 1,000 IMS head scans. Molds subjected to this test revealed no detectable wear of the mold-plate surface containing the cavities.

The future of IMS

Any new technology benefits from auspicious timing for its introduction. The convergence of flip-chip growth in a time of important transitions to Pb-free alloys and 300-mm wafers makes this an ideal time for a completely new bumping technology. Of the two, the transition to Pb-free alloys is surely producing the greatest challenges. Industry press reports have somewhat humorously drawn analogies between the pain of accepting Pb-free bumping realities and those of accepting the realities of death [17]. An introductory quote from Isaac Asimov sets the tone: "*Life is pleasant. Death is peaceful. It's the transition that's troublesome.*" And so it is with Pb-free bumping. It is both necessary and anticipated that the ideal Pb-free alloy and process will become mainstream, but at present the industry is going through that "troublesome transition." Gail Flowers, editor-in-chief of *Advanced Packaging* magazine, asked "*When will we see standardization in flip-chip processes? . . . What are the long shots in flip chips that could bring about major changes?*" [18]. A true industry-standard flip-chip bumping process that addresses the

Table 10 Pb-free bump data. From [8], reprinted with permission; © 2004 IEEE.

Wafer size (mm)	200	200
Chip size (mm)	14.7 × 14.7	14.7 × 14.7
Bumps per chip	2,452	2,452
Bumps per wafer	284,432	284,432
Bump pattern	Array	Array
Bump pitch (mils)	4 on 9	4 on 9
Wafer quantity	3	3
Pb-free alloy	Sn3.8Ag0.7Cu	Sn0.7Cu
Bump heights (μm)		
• Wafer mean	101.3	79.9
• Wafer sigma	2.7	2.8
• Chip sigma	1.7	2.3

painful transition can be a game-changer in a market that some industry analysts expect to increase from \$3.5 billion in 2003 to nearly \$8 billion in 2007. With this in mind, IBM and SUSS MicroTec AG of Munich, Germany, made a major announcement on September 13, 2004, unveiling the C4NP (controlled collapse chip connect new process) for Pb-free solder. SUSS is developing the toolset for the industry to enable C4NP technology, which is simply IMS applied to wafer bumping.

Some of the process steps described above may change owing to optimization for manufacturing. Also, IBM is continuing its advanced research on C4NP and offers on-site process training to customers interested in this new Pb-free enabling technology, all with the conviction that the multiple advantages of IMS address most if not all concerns regarding Pb-free wafer bumping in the industry.

While IMS is a potential new process for mainstream production, the work reviewed in this paper demonstrates that IMS technology in itself is not new, but rather has evolved, with considerable validation and scrutiny, to meet the foreseeable needs of wafer bumping. Time will show whether IMS can gain the market acceptance that is suggested by its attributes.

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